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Role of quantization effects in the operation of ultrasmall MOSFETs and SOI device structures

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Abstract

The continued scaling of devices towards the ultimate limit of 50-nm MOSFET by the year 2007 necessitates the use of higher substrate doping densities in both conventional devices and in the alternative device technologies. The higher substrate doping density, on the other hand, gives rise to pronounced space quantization effects that must be taken into account when modeling these novel device structures. One way to include space quantization is via solution of the Schrödinger equation coupled to conventional drift-diffusion, hydrodynamic or Monte Carlo particle-based simulators. An alternative way is to use the recently proposed effective potential approach. In this work, we apply the effective potential approach when modeling a conventional 50-nm MOSFET device and an SOI device structure. For the SOI device we also utilize the Landauer's approach to calculate the current and estimate the device threshold voltage increase due to the lateral quantization.

Keywords: Ultra-small MOSFETs; SOI devices; Quantization effects

1. Effective potential approach

The idea of quantum potentials originates from the hydrodynamic formulation of the quantum mechanics, first introduced by de Broglie and Madelung [1,2] and later developed by Bohm [3]. In this picture, the wave function is written in complex form in terms of its amplitude and phase $\psi(\mathbf{r},t) = R(\mathbf{r},t)\exp[iS(\mathbf{r},t)/\hbar]$. When substituted back into the Schrödinger equation, it leads to coupled equations of motion that have the form of the classical hydrodynamic equations with the addition of an extra potential, often referred to as the quantum or Bohm potential, written as

$$Q = -\frac{\hbar^2}{2mR}\nabla^2 R \rightarrow -\frac{\hbar^2}{2m\sqrt{n}}\cdot\frac{\partial^2\sqrt{n}}{\partial x^2} \tag{1}$$

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where the square root of the density n represents the magnitude of the wave function R. The Bohm potential is essentially a field through which the particle interacts with itself. It has been used, for example, in the study of wave-packet tunneling through barriers [4].

In analogy to the smoothed potential representation discussed above for the quantum hydrodynamic models, it is desirable to define a smooth quantum potential for use in quantum particle based simulation. Ferry [5] suggested an effective potential that is derived from a wave packet description of particle motion. Within this formulation, the effective potential V_{eff} is related to the self-consistent Hartree potential V, obtained from the Poisson equation, through an integral smoothing relation

$$V_{\text{eff}}(x) = \int V(x+y)G(y,a_0)\,\mathrm{d}y \tag{2}$$

where G is a Gaussian with standard deviation a_0. This effective potential V_{eff} is then used to calculate the electric field that accelerates the carriers in the transport simulator, described in more detail in [6]. The use of V_{eff} has a fairly low computational cost, i.e. $<10\%$ increase in CPU time.

2. Simulation results

2.1. Conventional MOSFET device

The first device structure to which we apply the effective potential scheme is a 50-nm MOSFET device, with channel doping of 10^{18} cm^{-3}, source/drain doping equal to 10^{19} cm^{-3} and junction depth of 36 nm. The oxide thickness is 2 nm and the device width is 0.8 μm. We find reduction in the electron density and charge setback of about 2 nm, in agreement with some previous studies [6,7]. These two factors give rise to the threshold voltage reduction of ~80 mV and on-state current degradation of about 20%. Both trends are schematically shown in Fig. 1a and b, where we plot the device transfer and output characteristics, respectively [6].

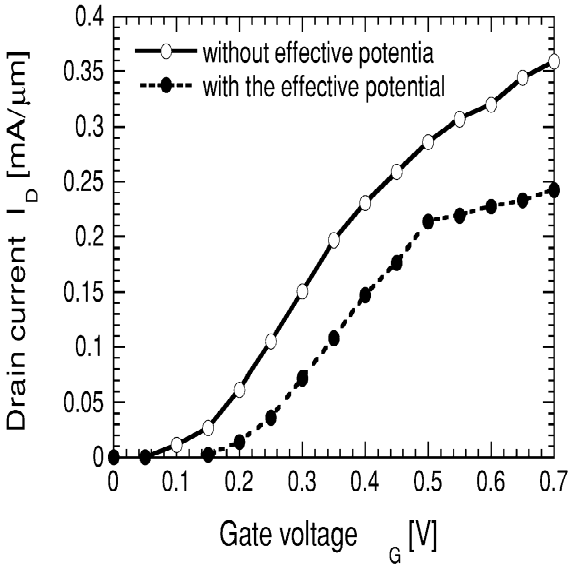
2.2. SOI device

The second device structure we simulate is a narrow channel silicon-on-insulator (SOI) device (see Fig. 2) that consist of a thick silicon substrate, on top of which 400 nm of buried oxide is grown. The thickness of the SOI layer is 7 nm, with p-region width between 5 and 15 nm. On top of the SOI layer sits the gate-oxide layer, the thickness of which is 34 nm.

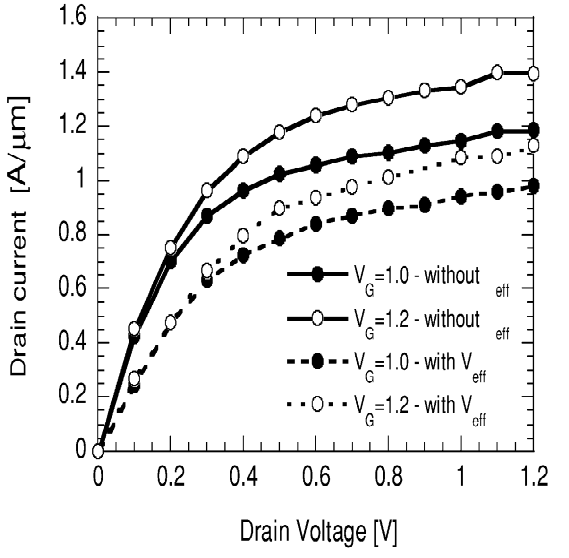
When modeling this device structure we employ two different methods

1. The effective potential approach in conjunction with the self-consistent solution of the 2D Schrödinger equation, to calculate the line electron density.
2. Use of the classical solution of the electrostatic confinement combined with the Landauer approach to calculate the on-state current as a function of the gate voltage.

The description of these two methods and the discussion of the simulation results obtained is given below.



(a)



(b)

Fig. 1. (a) Device transfer characteristics $V_d = 0.1$ V was used in these simulations. (b) Output characteristics of the device for two different values of the gates voltage.

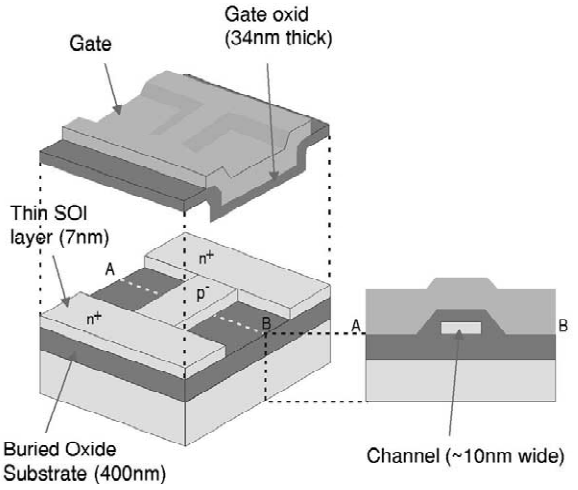


Fig. 2. Schematic description of the SOI device structure.

2.2.1. Effective potential approach versus self-consistent solution of the 2D Schrödinger equation

When solving the 2D Schrödinger equation, we have taken into account the pronounced mass anisotropy in the Si material system and the multivalley nature of the lowest conduction bands. Namely, the six conduction band valleys in Si are included through a standard three-valley model. Valley pair 1 points along the (100) direction having $m_x = m_l = 0.91m_0$ and $m_y = m_z = m_t = 0.19m_0$. Valley pair 2 points towards the (010) direction and has $m_x = m_z = m_t$ and $m_y = m_l$, and valley pair 3 points in the (001) direction, having $m_x = m_y = m_t$ and $m_z = m_l$. As a result of the above, at each iteration step, we solve the 2D Schrödinger equation, of the form

$$\left[-\frac{\hbar^2}{2m_y^{\nu}}\frac{\partial^2}{\partial y^2} - \frac{\hbar^2}{2m_z^{\nu}}\frac{\partial^2}{\partial z^2} + V(y,z) \right] \psi_j^{\nu}(y,z) = E_j^{\nu}\psi_j^{\nu}(y,z) \tag{3}$$

three times, i.e. for each equivalent valley pair ν. Once the energy eigenstates and the corresponding eigenfunctions are known, the electron density is found by using

$$n(y,z) = 2\sum_{\nu=1}^{3}\sum_{j} N_j^{\nu}\left|\psi_j^{\nu}(y,z)\right|^2 \tag{4}$$

where the factor of 2 accounts for valley degeneracy, the double sum represents summation over all energy eigenstates (index j) belonging to each of the three valley pairs (index ν) and the line charge density is given by

$$N_j^{\nu} = \frac{1}{\pi\hbar}\sqrt{2m_x^{\nu}k_B T}\cdot F_{-1/2}\left(\frac{E_F - E_j^{\nu}}{k_B T}\right) \tag{5}$$

where T is the temperature and k_B is the Boltzmann constant. In the actual evaluation of the Fermi–Dirac integral of order $-1/2$, which appears in Eq. (5), we use the approximate expression given in [8].

The calculated gate-voltage dependence of the line density, for the test device structure with

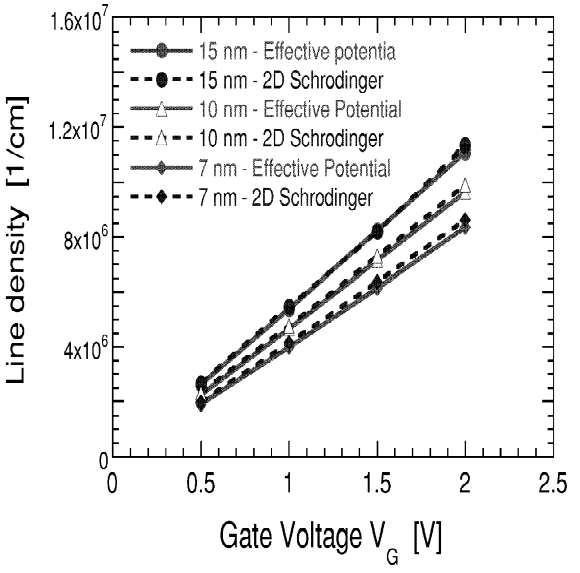


Fig. 3. Variation of the line charge density for a quantum wire that represents the channel region of the SOI device structure from Fig. 2. The wire width equals 7, 10 and 15 nm.

homogeneous confinement along the *x* axis, is shown in Fig. 3. For each wire width (7, 10 and 15 nm) we use both the effective potential approach discussed in Section 1, and the self-consistent solution of the 2D Schrödinger-3D Poisson problem. Excellent agreement is observed between the two approaches when using the theoretical value for the Gaussian smoothing parameter of 0.64 nm. This result suggests that the effective potential approach can be successfully used even for complicated confining potentials.

2.2.2. Classical solution combined with Landauer's formalism

Another approach to modeling the SOI device we discussed in Section 2.2 is to think of it as a quantum wire. This viewpoint is particularly useful in the ballistic regime, where most of the scattering comes from the device boundaries. As channel lengths become shorter, it becomes increasingly more appropriate to model devices in this manner.

A quantum wire is essentially a waveguide for propagating electron waves. Depending on the electron density and the width of the wire, only a certain number of quantized modes are allowed to propagate. The amount of current that is passed by the device then depends on the transmission probability of these modes. According to the formalism originally developed by Landauer [9] and extended by Büttiker [10], the source-drain current, I_D, can be expressed as the integral

$$I_D = \frac{2e}{h}\int [f(E) - f(E - eV_{DS})]\sum_{nm}|t_{nm}(E,V_{DS}, V_G)|^2 \, dE \tag{6}$$

where V_{DS} is the voltage drop from source to drain, $f(E)$ is the Fermi function for energy E, and t_{nm} is the transmission amplitude going from mode n to mode m, and the summation is over all propagating modes. Thus, obtaining the current comes down to computing these quantum mechanical transmission amplitudes. There are a number of different ways for doing this, but a method that we have used with

great success is that of Usuki et al. [11], who developed an approach based on numerically stabilized variant of the transfer matrix method. To begin, the Schrödinger equation is mapped onto a finite-difference mesh, on a square lattice of lattice constant a. Since the wires are of finite width, extending a given number (M) of lattice sites across, one can work in terms of slices, where ψ_j is an $\boldsymbol{M}$-dimensional vector containing the wave function amplitudes of the jth slice. The discretized Schrödinger equation, keeping terms up to first order in the approximation of the derivative, has the form:

$$(E - \boldsymbol{H}_j)\psi_j + \boldsymbol{H}_{j,j-1}\psi_{j-1} + \boldsymbol{H}_{j,j+1}\psi_{j+1} = 0 \tag{7}$$

In the above equation, the $\boldsymbol{H}_j$ matrices represent Hamiltonians for individual slices, and the matrices $\boldsymbol{H}_{j,j-1}$ and $\boldsymbol{H}_{j,j+1}$ give the inter-slice coupling. By approximating the derivative by a finite difference, the kinetic energy terms of Schrödinger's equation get mapped onto a tight-binding model with $t = -\hbar^2/2m^*a^2$ representing nearest neighbor hopping. The potential V at site i,j simply adds to the on-site energies, which appear along the diagonal of the $\boldsymbol{H}_j$ matrices. Transfer matrices, that allow translation from source to drain, can be derived using (7). These allow for the modes of the wire to be determined. Setting the boundary condition that these modes be occupied at the source end with unit amplitude, one obtains the transmission amplitudes that enter (6) by translating across the system. By using some clever matrix manipulations, Usuki overcame the problems created by the exponentially growing and decaying contributions of evanescent modes. Rather than just multiplying transfer matrices, the translation scheme is turned into an iterative procedure, which provides numerical stability by not allowing the evanescent contributions to diverge.

Simulation results for the device transfer characteristics, that utilize the above described approach, are shown in Fig. 4. The channel width is equal to 5, 7, 10 and 13 nm. We observe a drastic decrease

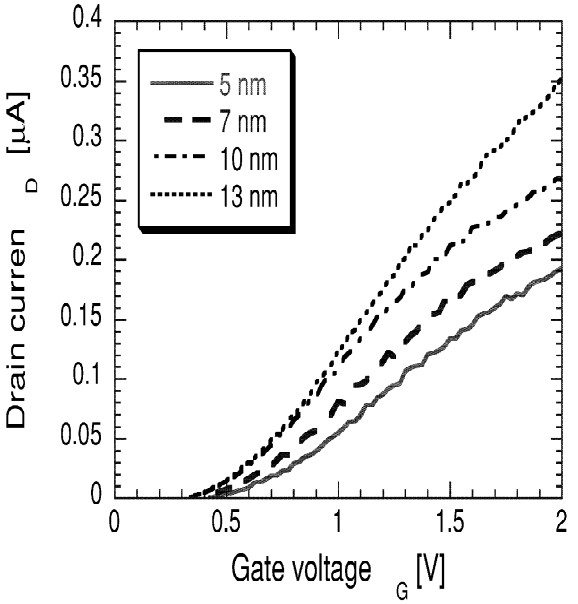


Fig. 4. Transfer characteristics of the SOI device with channel width equal to 5, 7, 10 and 13 nm. The drain voltage V_D equals 10 mV.

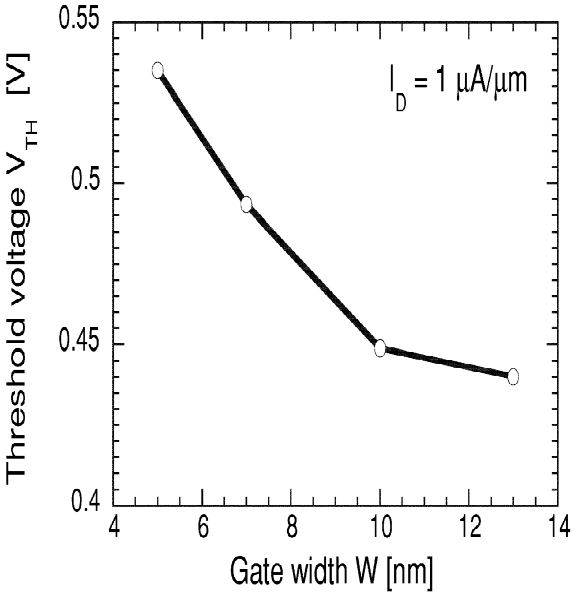


Fig. 5. Threshold voltage as a function of the gate width.

of the drain current with decreasing channel width due to the lateral space-quantization effect. This observation is seen more clearly from the results shown in Fig. 5, where we plot the device threshold voltage as a function of the channel width. Note that the threshold voltage equals the gate voltage for which the current equals 1 $\mu A/\mu m$.

3. Conclusions

In this paper, we utilized the effective potential approach to successfully account for quantization effects in a model of a 50-nm gate length MOSFET. The effective potential provides a setback of the charge from the interface, and a quantization energy within the channel. Both these effects lead to an increase in the threshold voltage, which is apparent in the output characteristics of the device. We also demonstrate that the effective potential approach can be successfully used in the case of more complicated confining potentials, such as the 2D confinement in the channel region of the SOI device from Fig. 2. For this particular device structure we found drastic increase in the threshold voltage width decreasing channel width.

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