Electron mobility in scaled silicon metal-oxide-semiconductor field-effect transistors on off-axis substrates

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Off-axis silicon wafers promise monolithic integration of III-V optoelectronics with silicon microelectronics. However, it is unclear how miniaturization affects electronic device performance on off-axis substrates. We present the fabrication and characterization of metal-oxide-semiconductor field-effect transistors (MOSFETs) with different gate lengths on regular Si(100) and 4° off-axis wafers. The field-effect electron mobility in the off-axis devices is lower than in their (100)-wafer counterparts with equivalent gate length. Monte Carlo simulations have reproduced the experimental data and demonstrated that the mobility degradation in off-axis devices stems from enhanced electron scattering from the Si/SiO_2 surface roughness. Short-channel MOSFETs on (100) and off-axis substrates perform comparably. © *2009 American Institute of Physics*.
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Silicon (100) substrates tilted a few degrees off axis enable growth of high-quality GaAs layers.[1] Therefore, it is possible to monolithically integrate GaAs optoelectronic devices (e.g., lasers) and silicon-based electronic devices [e.g., metal-oxide-semiconductor field-effect transistors (MOSFETs)].[2–4] Characteristics of MOSFETs fabricated on different primary silicon crystal planes have been studied previously.[5–8] The influence of the substrate rotation on MOSFET fabrication has also been investigated.[6,9,10] In all the previous work, differences in MOSFET performance on (100) and off-axis wafers have been reported, such as a lowering of the effective channel mobility and the mobility anisotropy.[6,10] As the MOS devices are fabricated on rotated substrates to integrate with III-V optoelectronics, while their dimensions keep scaling down, it becomes necessary to examine the influence that off-axis Si substrates have on the performance of MOSFETs with different channel lengths.

In this letter, we present the fabrication, characterization, and performance comparison of circular Si MOSFETs on regular (100) wafers and on off-axis wafers rotated by 4° around the [011] axis. Devices with gate lengths ranging from 10 down to 0.5 μm have been fabricated on the two substrates, and it has been found that the field-effect electron mobility of an off-axis MOSFET is lower than that of its normal (100) wafer counterpart of equivalent gate length. Using ensemble Monte Carlo (EMC) simulations, we demonstrate that the mobility degradation can be explained by an enhancement in the surface roughness scattering of electrons at the Si/SiO_2 boundary in off-axis substrates.[11] However, the mobility difference between devices on the two substrates decreases with decreasing gate length, and below the 1 μm mark the devices on the two substrates perform comparably. This finding bodes well for the prospects of integration of scaled-down high-performance Si electronics with high-performance III-V optoelectronics.

The substrates used in this study are lightly boron-doped ($\approx 5\times10^{14}$ cm^{-3}), *p*-type silicon (100) wafers and off-axis wafers rotated by 4° around the [011] axis. Atomic steps along the wafer cut line are formed on the off-axis wafer surface.[10] Circular MOSFETs of various gate lengths were fabricated on regular and 4° off-axis Si wafers. Figure 1 shows an optical microscope image and a scanning electron microscope (SEM) image (inset of Fig. 1) of a finished MOSFET. The fabrication process begins with the 40 nm thermal gate oxide growth (the oxide thickness is measured by Filmetrics F20 reflectometer, as well as by Alpha-step 200 profilometer, and is virtually identical in the two wafers, the difference being below 0.5 nm). SEM and electron-beam lithography are then employed to pattern the circular gates with various gate lengths, from 10 down to 0.5 μm. A 10/90 nm Ti/Au layer is evaporated at room temperature as the gate electrode. Then both regular and 4° off-axis substrates receive an *n*-type phosphorus source/drain (S/D) implantation with the energy of 70 keV, followed by rapid thermal annealing. The gate is used to self-align ion implantation. After implantation, the source and drain region electrodes are patterned upon careful alignment with the gate; buffered hydrofluoric acid (HF) is employed to remove the oxide on the S/D regions and finally a 10/120 nm Ti/Au layer is evaporated for

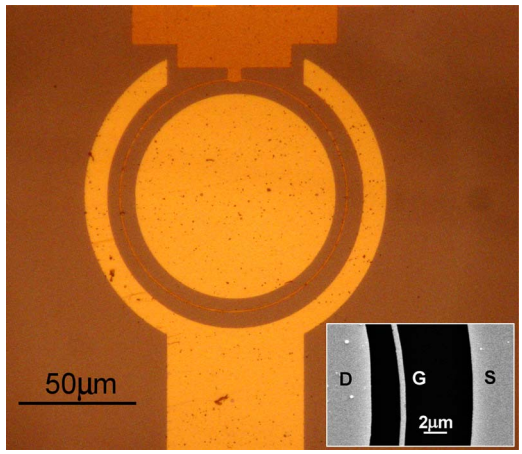

FIG. 1. (Color online) Optical microscope image of a circular MOSFET device (L_G=0.5 μm). Inset: SEM image of the MOSFET gate region.

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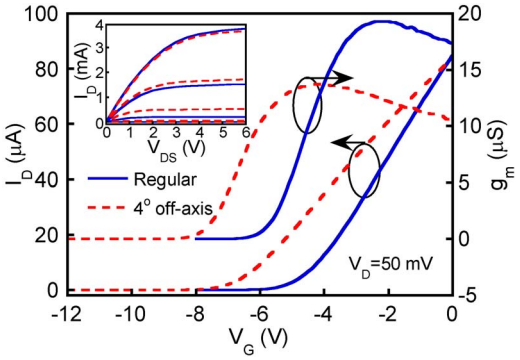

FIG. 2. (Color online) Comparison of the measured dc characteristics of MOSFETs with L_G=10 μm and W_G=320 μm fabricated on the regular (100) Si substrate (blue solid curves) and 4° off-axis Si substrate (red dashed curves). Linear transfer characteristics (V_D=50 mV) are presented in the main panel, while the inset features the I_D–V_{DS} curves (V_G=−6 to 0 V; the step between successive curves is 2 V).

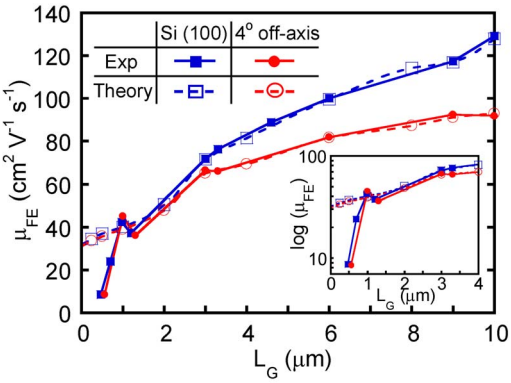

FIG. 3. (Color online) Effective channel mobilities of MOSFETs on the regular (100) substrate (blue curves) and 4° off-axis substrate (red curves) as a function of the gate length, from the calculation (dashed curves) and the experiment (solid curves). The mobility curve for the normal Si(100) wafer was obtained using the rms height of Δ=5 Å and the correlation length of λ=4 nm (blue dashed curve), while the parameters used for the off-axis substrate were Δ=5.4 Å and λ=4.3 nm (red dashed curve). For clarity, a semilog plot of the electron mobility in shorter channel devices is presented in the inset.

the S/D electrodes. Identical fabrication processes on both substrates and the circular-shape gate of the MOSFETs enable us to perform a comparison between devices independent of the channel orientation and thus the 4° off-axis substrate orientation is the only difference. The MOSFET gate width is also kept the same—all circular gates have the same diameter of 100 μm.

Figure 2 shows the dc characteristics comparison between the MOSFETs with gate length L_G=10 μm on regular and 4° off-axis Si substrates. The threshold voltage V_{th} is lower by about 2 V in the off-cut MOSFET. The downward shift of V_{th} is a trend we observed regardless of the gate length, and it has two likely causes: (1) Self-aligned ion implantation is performed at 7° angle to minimize channeling. While this angle is optimal for (100) wafers, it is likely not for the off-axis wafer. Therefore, we expect more dopant diffusion into the channel in off-axis devices, so the effective channel doping is probably higher than the nominal doping value (roughly 5×10^{14} cm^{-3}) and V_{th} becomes more negative. (2) Interface trap density is expected to be higher at the Si/SiO_2 interface in off-axis wafers.[12] In the inset of Fig. 2, the I_D-V_{DS} curves for the two MOSFETs are depicted, as the gate bias is swept from −6 to 0 V with an increment of 2 V. Due to the large threshold voltage offset, same-V_G curves in the two devices actually correspond to very different stages of inversion.

In Fig. 2, we also see that the device on the off-axis substrate has a significantly lower transconductance, which infers that its field-effect channel mobility is lower. Experimentally obtained field-effect electron mobility (μ_{FE}), extracted from the peak measured transconductance, is shown in Fig. 3 as a function of the gate length for MOSFETs on the regular (100) substrate (blue solid curve) and the 4° off-axis substrate (red solid curve). The relatively low field-effect mobility values of the fabricated MOSFETs are due to unoptimized device doping profiles.[13,14] However, our focus here is on comparing the MOSFET performances on the two substrates under identical fabrication conditions rather than on optimization.

Chung *et al.*[10] observed lowering and anisotropy of the electron mobility in devices on rotated wafers and argued that there are two interwoven causes for this behavior: The anisotropy of the conductivity mass in off-axis wafers and the different surface roughness scattering along and across the (100) steps.[9,10] Since our MOSFET channels are circular, we measure a mobility value averaged over the electric field direction. The effective conductivity mass for radially symmetric carrier transport and small 4° misorientation will be identical to the usual conductivity mass for (100), so the remaining reason for a lower mobility than on the (100) substrate is surface roughness scattering. Two additional phenomena could in principle affect the mobilities in the two wafers differently, but are negligible for the situation at hand: (1) Valley splitting between conduction band minima due to tilting[15] is smaller than 0.1 meV for the 4° misorientation, and can be neglected in room-temperature transport. (2) The effective channel doping level due to additional dopant diffusion in off-axis devices is probably not high enough (it would have to exceed 10^{17} cm^{-3}) to significantly alter the electron mobility.

We therefore assert that the mobility degradation in our circular gate MOSFETs on the off-axis substrate occurs due to an effective enhancement in the rate of electron scattering with the Si/SiO_2 surface roughness. To support the hypothesis, we simulated electron transport in MOSFETs using two-dimensional EMC.[16] The roughness is described by an exponential autocovariance function, $\langle\delta(\boldsymbol{r})\delta(\boldsymbol{r}-\boldsymbol{r}')\rangle = \Delta^2 e^{-\sqrt{2}r'/\lambda}$, where $\delta(\boldsymbol{r})$ is a local deviation of the Si/SiO_2 boundary position from a perfect plane as a function of the in-plane coordinate $\boldsymbol{r}$, Δ is the rms value of $\delta(\boldsymbol{r})$, and λ is the correlation length.[11] Electrons in the simulation hit the rough Si/SiO_2 interface and bounce back specularly. So, for given Δ and λ, we generate a random rough surface by employing a fast Fourier transform method proposed by Wu,[17] and we simulate the transport in MOSFETs with gate lengths ranging from 0.25 to 10 μm. The mobility is extracted from the numerically obtained linear-regime transconductance, in order to match closely the procedure used in the experiment.

Figure 3 shows a very good agreement between the measured (solid curves) and calculated (dashed curves) electron mobilities as a function of the gate length for MOSFETs on regular (blue curves) and 4° off-axis substrates (red curves). The calculated mobility curves were obtained using roughness parameters Δ=5 Å and λ=4 nm for the (100) substrate, and Δ=5.4 Å and λ=4.3 nm for the off-axis sub-

strate. The rms heights are somewhat higher than the typical values used for dry oxidation, consistent with the use of wet oxidation during the fabrication. Intuitively, a larger Δ in off-axis wafers can be linked to the existence of the relatively high (100) steps.

The mobility in both theory and experiment decreases with decreasing gate length, owing to two reasons: (1) Parasitic S/D series resistances that lead to transconductance lowering, and unless accounted for explicitly, will result in a lower mobility extracted.[14] However, parasitics in our theory are negligible (short and highly doped S/D) and the same trend persists, which leads us to the second reason that governs mobility drop with decreasing L: (2) Limitations of the common approximation used to relate transconductance g_m to the channel mobility for $V_{DS} \ll V_G - V_{th}$: $\mu_{FE} = g_m / C_{ox} V_{DS}(L/W)$, where C_{ox} is the oxide capacitance and L and W are the gate length and width. The underlying assumptions are that the total inversion sheet charge density Q_{inv} is independent of L and equals $C_{ox}(V_G - V_{th})$, while the electric field along the channel is constant and equals to $E_{\|} = V_{DS}/L$. In reality, for fixed $V_G - V_{th}$ and V_{DS}, total inversion sheet charge density $Q_{inv} \leq C_{ox}(V_G - V_{th})$ decreases with decreasing L. Also, the product of the local sheet charge density $en_s(x)$ and the parallel electric field $E_{\|}(x)$ integrated along the channel $e\int_0^L n_s(x)E_{\|}(x)\mathrm{d}x$ is generally smaller than $C_{ox}(V_G - V_{th})V_{DS}$. Therefore, by using the above relationship between the mobility and transconductance, we end up extracting a mobility value different from the "real" one by roughly a factor of $e\int_0^L n_s(x)E_{\|}(x)\mathrm{d}x / C_{ox}(V_G - V_{th})V_{DS} < 1$ that drops with decreasing L.

At gate lengths below about 1 μm, there is a discrepancy between the calculated and measured mobilities in both wafers. One reason is that the source and drain series resistances become comparable to the channel resistance and drag the transconductance below the theoretical value that accounts for the channel resistance alone. Another issue is that smaller MOSFETs suffer more from channel shortening due to dopant diffusion during annealing and exhibit poorer gate control over the channel (e.g., drain-induced barrier lowering and even punchthrough for $L_G < 0.25$ μm). Due to the latter, the transconductance also drops and the extracted mobility appears lower than the theoretical estimate. Furthermore, with short-channel devices, the uniformity of the gate metallization coverage and device yield become more problematic. Fluctuations, such as the dip and the peak in the measured mobility around $L_G = 1$ μm (Fig. 3) are observed because of very few available working devices to average over.

The mobility difference decreases with decreasing gate length, starting at about 40 $\mathrm{cm}^2/\mathrm{Vs}$ for $L_G = 10$ μm and becomes negligible in devices with gate lengths below $L_G = 2$ μm. (For clarity, the mobility in shorter-channel devices is depicted on a semilog scale in the inset of Fig. 3.) The decrease in the mobility difference is consistent with surface roughness scattering as the dominant difference in transport on the two substrates: as the channel gets shorter while V_G-V_{th} and V_{DS} are kept constant, Q_{inv} and the average effective field from the gate decrease. The average distance of carriers from the rough surface slowly increases (the channel gets "thicker") and a smaller percentage of carriers scatter strongly form the rough Si/SiO_2 boundary, so the mobility difference due to surface roughness scattering drops.

In summary, circular MOSFETs with gate lengths from 10 down to 0.5 μm were fabricated on regular (100) Si and 4° off-axis Si substrates. MOSFETs on the regular (100) substrate have higher mobilities than their counterparts on the 4° off-axis substrate, but the mobility difference between the two MOSFETs with the same gate length decreases with decreasing gate length. Simulation demonstrates that surface roughness scattering is the underlying mechanism for the different characteristics on regular and off-axis substrates. MOSFETs with small gate length perform comparably on 4° off-axis and (100) Si substrates. The results unveil opportunities for employing small-angle off-axis Si wafers for monolithic integration of high-performance scaled Si microelectronics with compound semiconductor optoelectronics, without a significant degradation in the electronic device performance.

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